ANNA UNIVERSITY, CHENNAI

UNIVERSITY DEPARTMENTS

REGULATIONS - 2023

M.E. VLSI DESIGN

VISION

The Department of ECE shall strive continuously to create highly motivated, technologically competent engineers, be a benchmark and a trend setter in Electronics and Communication Engineering by imparting quality education with interwoven input from academic institutions, research organizations and industries, keeping in phase with rapidly changing technologies imbibing ethical values.

MISSION

- Imparting quality technical education through flexible student centric curriculumevolved continuously for students of ECE with diverse backgrounds.
- Providing good academic ambience by adopting best teaching and learningpractices.
- Providing congenial ambience in inculcating critical thinking with a quest forcreativity, innovation, research and development activities.
- Enhancing collaborative activities with academia, research institutions andindustries by nurturing ethical entrepreneurship and leadership qualities.
- Nurturing continuous learning in the stat-of-the-art technologies and globaloutreach programmes resulting in competent world class engineers.

PROGRAMME EDUCATIONAL OBJECTIVES:

1. Teach students to understand the principles involved in the latest technology and software required to design and critically analyze the Chip Design relevant to industry and society
2. Blend theory and laboratory to make students appreciate the concepts in the working of Chip Design.
3. Mould the students to progress and develop with ethics and to communicate effectively
4. Motivate students to take up socially relevant and challenging projects and propose innovative solutions to problems for the benefit of the society
5. To motivate students to become entrepreneurs to develop indigenous solutions.

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PROGRAM OUTCOMES:

PO#	Graduate Attribute	Programme Outcome
1.	Research aptitude	An ability to independently carry out research/investigation and development work to solve practical problems
2.	Technical documentation	An ability to write and present a substantial technical report/document
3.	Technical competence	Students should be able to demonstrate a degree of mastery over VLSI Design and Analysis.
4.	Engineering Design	An ability to apply **advanced** concepts of VLSI for chip design with state of art tools
5.	The engineer and society	An ability to **evolve** customizable Chip Design for different Engineering applications
6.	Environment and sustainability	An ability to provide paradigm solution in the development of **customized** prototypes and chip design which have social and global **relevance**

MAPPING OF PROGRAMME EDUCATIONAL OBJECTIVES WITH PROGRAMMEOUTCOMES:

A broad relation between the programme objective and the outcomes is given in the following table:

PEOs	Programme Outcomes					
	PO1	PO2	PO3	PO4	PO5	PO6
1	3	3	3	3		
2	2	2	2	2		
3					2	3
4					3	3
5	3	3	3	3	3	2

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YEAR	SEM	COURSE TITLE	PO1	PO2	PO3	PO4	PO5	PO6
YEAR 1	SEMESTER 1	Semiconductor Device Modeling and Simulation	3	1.3	3	3	2.8	
		Digital CMOS VLSI Design	1.75		2.5	2.2	1	
		Analog Integrated Circuit Design	3	2.3	3	3	1	
		VLSI Digital Signal Processing	3		3	2.8	1	
		Hardware Description Languages for RTL Designs	1.75	2.5	2.5	1.75	1	
		Research Methodology and IPR						
	SEMESTER 2	Data Converters IC Design	3		3	2.8	1	
		Low Power VLSI Design	3	2.3	3	3	1	
		Multi-core Architecture & ISA Verification	1.75		2.5	2.2	1	
		Professional Elective I						
		Professional Elective II						
		PCB Design and Assembly Lab		1	2.5	2.6	2	2
		Idea to Product (VLSI Subsystem Design)	1	1	2	2.4	1	
YEAR 2	SEMESTER 3	Professional Elective III						
		Professional Elective IV						
		Professional Elective V						
		Project Work I						
	SEMESTER 4	Project Work II						

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UNIVERSITY DEPARTMENTS

REGULATIONS - 2023

M.E. VLSI DESIGN

CURRICULA AND SYLLABI

SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL3101	Semiconductor Device Modelling and Simulation	FC	2	0	2	4	3
2.	RM3151	Research Methodology and IPR	MC	2	1	0	3	3
3.	VL3151	Digital CMOS VLSI Design	PCC	3	0	0	3	3
4.	AP3151	Analog Integrated Circuit Design	PCC	3	0	4	7	5
5.	VL3102	VLSI Digital Signal Processing	PCC	3	0	0	3	3
6.	VL3103	Hardware Description Languages for RTL Designs	PCC	3	0	4	7	5
			TOTAL	**16**	**1**	**10**	**27**	**22**

SEMESTER II

SL. NO	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL3201	Data Converters IC Design	PCC	3	0	0	3	3
2.	VL3202	Low Power VLSI Design	PCC	3	0	4	7	5
3.	VL3203	Multi-Core Architecture and ISA Verification	PCC	3	0	0	3	3
4.		Professional Elective I	PEC	3	0	0	3	3
5.		Professional Elective II	PEC	3	0	0	3	3
PRACTICAL								
6.	VL3211	PCB Design and Assembly Laboratory	PCC	0	0	4	4	2
7.	VL3212	Idea to Product (VLSI Subsystem Design)	EEC	0	0	4	4	2
			TOTAL	**15**	**0**	**12**	**27**	**21**

SEMESTER III

SL. NO	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1		Professional Elective III	PEC	3	0	0	3	3
2		Professional Elective IV	PEC	3	0	0	3	3
3		Professional Elective V	PEC	3	0	0	3	3
PRACTICAL								
4	VL3311	Project Work I	EEC	0	0	12	12	6
			TOTAL	**9**	**0**	**12**	**21**	**15**

SEMESTER IV

SL. NO	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICAL								
1	VL3411	Project Work II	EEC	0	0	24	24	12
TOTAL				**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS: 70

FOUNDATION COURSES (FC)

SL. NO	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL3101	Semiconductor Device Modeling and Simulation	FC	2	0	2	4	3

PROFESSIONAL CORE COURSES (PCC)

SI. NO	COURSE CODE	COURSE TITLE	CATE GORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL3151	Digital CMOS VLSI Design	PCC	3	0	0	3	3
2.	AP3151	Analog Integrated Circuit Design	PCC	3	0	4	7	5
3.	VL3102	VLSI Digital Signal Processing	PCC	3	0	0	3	3
4.	VL3103	Hardware Description Languages for RTL Designs	PCC	3	0	4	7	5
5.	VL3201	Data Converters IC Design	PCC	3	0	0	3	3
6.	VL3202	Low Power VLSI Design	PCC	3	0	4	7	5
7.	VL3203	Multi-core Architecture & ISA Verification	PCC	3	0	0	3	3

8.	VL3211	PCB Design and Assembly Laboratory	PCC	0	0	4	4	2

PROFESSIONAL ELECTIVE COURSE (PEC)

Sl. No.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	CONTACT PERIODS	CREDITS
1	AP3058	Wireless Sensor Networks	PEC	3	0	0	3	3
2	VL3001	PCB Circuit Design	PEC	3	0	0	3	3
3	AP3051	Advanced Microprocessors and Microcontrollers	PEC	3	0	0	3	3
4	AP3052	Electronics for Solar Power	PEC	3	0	0	3	3
5	AP3056	Robotics and Intelligent Systems	PEC	3	0	0	3	3
6	VL3002	RF System Design	PEC	3	0	0	3	3
7	AP3057	Signal Integrity for High Speed Design	PEC	3	0	0	3	3
8	AP3053	EMI and EMC in System Design	PEC	3	0	0	3	3
9	VL3003	Hardware and Software Co-Design	PEC	3	0	0	3	3
10	VL3004	Reconfigurable Computing	PEC	3	0	0	3	3
11	VL3005	Evolvable Hardware	PEC	3	0	0	3	3
12	VL3006	Power Management and Clock Distribution Circuits	PEC	3	0	0	3	3
13	VL3007	Testing of VLSI Circuits	PEC	3	0	0	3	3
14	VL3008	SoC Design	PEC	3	0	0	3	3
15	VL3051	ASIC Design	PEC	3	0	0	3	3
16	VL3009	CAD for VLSI Circuits	PEC	3	0	0	3	3
17	VL3010	Advanced Signal Processing	PEC	3	0	0	3	3
18	AP3251	Advanced Digital System Design	PEC	3	0	0	3	3
19	VL3052	Fundamentals of Spintronics and Quantum Computing	PEC	3	0	0	3	3
20.	VL3055	Neuromorphic Computing	PEC	3	0	0	3	3
21.	VL3053	Machine Learning in VLSI Design	PEC	3	0	0	3	3
22.	VL3054	MEMS and NEMS	PEC	3	0	0	3	3
23.	VL3011	Mixed Signal IC Design	PEC	3	0	0	3	3

RESEARCH METHODOLOGY AND IPR COURSES (RMC)

S. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS	SEMESTER
			L	T	P		
1.	RM3151	Research Methodology and IPR	2	1	0	3	1
TOTAL CREDITS						3	

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EMPLOYABILITY ENHANCEMENT COURSES (EEC)

SI.NO	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL3212	Idea to Product (VLSI Subsystem Design)	EEC	0	0	4	4	2
2.	VL3311	Project Work I	EEC	0	0	12	12	6
3.	VL3411	Project Work II	EEC	0	0	24	24	12

Summary Credit Distribution for Various Category of Course by Semester Wise

M.E. VLSI DESIGN						
S.No	Subject Area	Credits per Semester				Credits Total
		I	II	III	IV	
1	FC	3				3
2	PCC	16	13			29
3	PEC		6	9		15
4	MC	3				3
5	EEC		2	6	12	20
	Total	22	21	15	12	70

VL3101 SEMICONDUCTOR DEVICE MODELING AND SIMULATION L T P C
2 0 2 3

UNIT I BASIC THEORY OF SEMICONDUCTORS 6

Introduction, - direct and indirect semiconductors – Fermi-Dirac statistics - Quasi-Fermi Levels - Poisson's Equation, conduction in semiconductor, effect of temperature, doping, and high electric field on carrier mobility, PN junction at equilibrium - current-voltage characteristics-diode current model and its limitations

UNIT II MOSFET DEVICE PHYSICS 6

MOS capacitor – potential balance and charge balance, the effect of gate-body voltage – MOSFET structures - qualitative description of MOS transistor operation – MOS transistor characteristics – Transistor regions of operations – CMOS fabrication process.

UNIT III MOSFET STATIC MODELS 6

Static drain current model – simple charge control model - Pao-Sah model - Pierret-Shields's model – charge sheet model – strong inversion model – weak inversion model – SPICE model, short channel effects, Quantum mechanical effects, modeling of lightly doped drain MOSFET and SOI MOSFET.

UNIT IV MODELING FOR CIRCUIT SIMULATORS 6

Introduction, types of models, attributes for good compact models, model formulation, model implementation in circuit simulators, model testing, parameter extraction, simulation, and extraction for RF applications, compact models – BSIM models - EKV models – PSP models.

UNIT V DEVICE SCALING AND VARIABILITY EFFECTS 6

Introduction, classical scaling laws, process variability- global and local process variability, characterization of parametric variability in MOSFETs, Reliability of MOSFETs - high-field effects, hot carrier degradation, bias temperature instability, MOSFET breakdown, high-k dielectrics.

TOTAL: 30 PERIODS

LAB EXPERIMENTS:

Simulations using MATLAB/TCAD/Equivalent Open-Source tools

1. Simulation of transfer characteristics (I_{DS} vs V_{GS}) of MOSFET
2. Simulation of drain characteristics (I_{DS} vs V_{DS}) of MOSFET
3. Extraction of threshold voltage, transconductance, device ON and OFF current, and subthreshold slope of MOSFET
4. Numerical simulation of drain current characteristics of MOSFET

Simulations using SPICE tools

5. Simulation of transfer and drain characteristics of NMOS and PMOS transistors using Verilog-A based BSIM4 models
6. Simulation of voltage transfer characteristics of CMOS inverter using Verilog-A based BSIM SOI models
7. Simulation of short channel effects such as threshold voltage roll-off and DIBL effects of nano-scaled MOSFET using the model card
8. Simulation of variations of MOSFET transfer characteristics due to process variability effects

9. Simulation of NMOS transistors incorporating the hot-carrier effects using sub-circuit modules
10. Simulation of PMOS transistors incorporating the negative bias temperature instability using sub-circuit modules

TOTAL: 60 PERIODS

COURSE OUTCOMES:

At the end of the course, the student will be able to:

CO1:Apply the semiconductor concepts of drift, diffusion, donors and acceptors, majority and minority carriers, and carrier mobility
CO2: Illustrate the physics and principles of operation of p-n junction diodes, MOS capacitors, and MOSFETs
CO3: Design and simulate MOSFET devices, taking into consideration of non-ideal and short-channel effects
CO4: Develop compact models for short-channel MOSFETs suitable for SPICE simulators
CO5:Analyze the process variability and reliability effects of the nano-scaled MOSFETs and simulate the device lifetime.

REFERENCES:

1. Tsividis, Y. & McAndrew, C. Operation, and modeling of the MOS transistor. Third edition, Oxford University Press, USA: 2011.
2. AB Bhattacharyya, “Compact MOSFET models for VLSI design”, Wiley, New York, 2009.
3. J.J. Liou, A. Ortiz-Conde, F. Garcia-Sanchez, “Analysis and Design of MOSFETs: Modeling, Simulation, and Parameter Extraction”, Springer Science & Business Media, 1998.
4. K. Saha, “Compact models for integrated circuit design: Conventional transistors and beyond”, Taylor & Francis, 2015**.**
5. T. Ytterdal, Y. Cheng, T. A. Fjeldly, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons, New York 2003.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	1	3	2	1	
CO2	3	1	3	3	1	
CO3	3	1	3	3	1	
CO4	3	1	3	3	1	
CO5	3	1	3	3	1	
AVG	3	3	3	3	1	

RM3151 RESEARCH METHODOLOGY AND IPR L T P C
2 1 0 3

UNIT I RESEARCH PROBLEM FORMULATION 9

Objectives of research, types of research, research process, approaches to research; conducting literature review- information sources, information retrieval, tools for identifying literature, Indexing

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and abstracting services, Citation indexes, summarizing the review, critical review, identifying research gap, conceptualizing and hypothesizing the research gap

UNIT II RESEARCH DESIGN AND DATA COLLECTION 9

Statistical design of experiments- types and principles; data types & classification; data collection - methods and tools

UNIT III DATA ANALYSIS, INTERPRETATION AND REPORTING 9

Sampling, sampling error, measures of central tendency and variation,; test of hypothesis- concepts; data presentation- types of tables and illustrations; guidelines for writing the abstract, introduction, methodology, results and discussion, conclusion sections of a manuscript; guidelines for writing thesis, research proposal; References – Styles and methods, Citation and listing system of documents; plagiarism, ethical considerations in research

UNIT IV INTELLECTUAL PROPERTY RIGHTS 9

Concept of IPR, types of IPR – Patent, Designs, Trademarks and Trade secrets, Geographical indications, Copy rights, applicability of these IPR; , IPR & biodiversity; IPR development process, role of WIPO and WTO in IPR establishments, common rules of IPR practices, types and features of IPR agreement, functions of UNESCO in IPR maintenance.

UNIT V PATENTS 9

Patents – objectives and benefits of patent, concept, features of patent, inventive steps, specifications, types of patent application; patenting process - patent filling, examination of patent, grant of patent, revocation; equitable assignments; Licenses, licensing of patents; patent agents, registration of patent agents.

TOTAL: 45 PERIODS

COURSE OUTCOMES

Upon completion of the course, the student can

CO1: Describe different types of research; identify, review and define the research problem

CO2: Select suitable design of experiment s; describe types of data and the tools for collection of data

CO3: Explain the process of data analysis; interpret and present the result in suitable form

CO4: Explain about Intellectual property rights, types and procedures

CO5: Execute patent filing and licensing

REFERENCES:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Soumitro Banerjee, “Research methodology for natural sciences”, IISc Press, Kolkata, 2022,
3. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
4. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

VL3151 **DIGITAL CMOS VLSI DESIGN** **L T P C**
3 0 0 3

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Stick diagram and Layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Nonbistable Sequential Circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs

UNIT V MEMORY ARCHITECTURES 6

Memory Architectures and Memory control circuits : Read-Only Memories, ROM cells, Read- write memories (RAM), dynamic memory design, 6 transistor SRAM cell, Sense amplifiers.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: To be able to use mathematical methods and circuit analysis models in analysis of CMOS digital circuits

CO2:To be able to create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort

CO3:To be able to design sequential logic at the transistor level and Compare the tradeoffs of sequencing elements including flip-flops, transparent latches

CO4:To be able to learn design methodology of arithmetic building blocks

CO5:To be able to design functional units including ROM and SRAM

REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B Nikolic, “Digital Integrated Circuits: A Design Perspective”, Prentice Hall of India, 2nd Edition, May 2016,
2. N.Weste, K. Eshraghian, “ Principles of CMOS VLSI Design”, Addison Wesley, 2nd Edition, 1993
3. M J Smith, “Application Specific Integrated Circuits”, Addison Wesley, January 2002.
4. Sung-Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and Design”, McGraw-Hill, December 2002.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1			1	1	
CO2	1		2	1	1	

CO3	1			1	1	
CO4	1		2	1	1	
CO5	1			1	1	
Avg.	1		2	1	1	

AP3151 ANALOG INTEGRATED CIRCUIT DESIGN L T P C

3 0 4 5

UNIT I SINGLE STAGE AMPLIFIERS 9

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower differential with active load, Cascode and folded Cascode configurations with active load, Design of differential and Cascode amplifiers – to meet specified SR, gain, BW, ICMR and power dissipation, voltage swing, High gain amplifier, structures.

UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OFAMPLIFIERS 9

Miller effect, association of poles with nodes, frequency response of CS, CG and sourcefollower, Cascode and differential pair stages, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III NEGATIVE FEEDBACK AMPLIFIERS AND OPERATIONAL AMPLIFIERS 9

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, One-stage OpAmps, Two-stage OpAmps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in OpAmps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE OPERATIONAL AMPLIFIER 9

Analysis of two stage OpAmp – two stage OpAmp single stage CMOS CS as second stage and using Cascode second stage, multiple systems, Phase Margin, Frequency Compensation, and Compensation of two stage OpAmps, Slewing in two stage OpAmps, Other compensation techniques.

UNIT V VOLTAGE AND CURRENT REFERENCES 9

Current sinks and sources, Current mirrors, Wilson current source, Widlar current source, Cascode current source, Design of high swing Cascode sink, current amplifiers, Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing.

TOTAL: 45 PERIODS

PRACTICAL EXERCISES:

1. Extraction of process parameters of CMOS process Transistors
    a. Plot ID vs. VGS at different drain voltages for nMOS, PMOS.
    b. Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
    c. Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and

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determine IOFF and sub-threshold slope.

d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.

2. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.
    a. Calculate input bias voltage for a given bias current.
    b. Use spice and obtain the bias current. Compare with the theoretical value
    c. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in spice, considering load capacitance.
    d. Plot step response of the amplifier with a specific input pulse amplitude. Derive time constant of the output and compare it with the time constant resulted from -3dB BW.
    e. Use spice to determine input voltage range of the amplifier.
3. Realize layout and perform post layout simulation of the CS amplifier realized in Ex.No.2
4. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter
    a. Perform DC analysis and determine input common mode range and compare with the theoretical values.
    b. Perform time domain simulation and verify low frequency gain.
    c. Perform AC analysis and verify low-frequency voltage gain and unity gain BW (fu)
5. Stability Analysis of Two stage OpAmp
    a. Perform DC analysis and determine input common mode range and compare with the theoretical values.
    b. Perform time domain simulation and verify low frequency gain.
    c. Perform AC analysis and verify low-frequency voltage gain and unity gain BW (fu)

TOTAL: 60 PERIODS

COURSE OUTCOMES:

CO1: Ability to design amplifiers to meet user specifications
CO2: Ability to analyse the frequency and noise performance of amplifiers
CO3: Ability to design and analyse negative feedback amplifiers and opAmps
CO4: Ability to analyse stability aspects of two stage opAmps
CO5: Ability to design and use current mirrors, current sources using MOS devices

REFERENCES:

1. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2nd Edition, 2016.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, March 2007.
3. Grebene, “Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons,Inc.,2003.
4. Phillip E.Allen, Douglas R.Holberg, “CMOS Analog Circuit Design”, Oxford University Press, 3rd October 2013.
5. Recorded lecture available at http://www.ee.iitm.ac.in/~ani/ee5390/index.html
6. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation, Third Edition”, WileyIEEE Press, 4th Edition,August 2019.

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Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	3	3	1	
CO2	3	3	3	3	1	
CO3	3	1	3	3	1	
CO4	3	1	3	3	1	
CO5	3	1	3	3	1	

VL3102 VLSI DIGITAL SIGNAL PROCESSING L T P C
3 0 0 3

UNIT I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING OF FIR FILTERS 9

Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, Longest path matrix algorithm,Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, propertiesof unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank- order filters.

UNIT III FAST CONVOLUTION, PIPELINING AND PARALLEL PROCESSING OF IIR FILTERS 9

Fast convolution – Cook-Toom algorithm, modified Cook-Toom algorithm, Pipelined and parallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2 decomposition, Clustered look-ahead pipelining, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry ripple and carry-save multipliers, Design of Lyon‟s bit-serial multipliers using Horner‟s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

UNIT V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Numerical strength reduction – sub expression elimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to determine the parameters influencing the efficiency of DSP architectures andapply pipelining and parallel processing techniques to alter FIR structures for efficiency

CO2: Ability to analyse and modify the design equations leading to efficient DSP architectures for transforms

CO3: Ability to speed up convolution process and develop fast and area efficient IIR structures

CO4: Ability to develop fast and area efficient multiplier architectures

CO5: Ability to reduce multiplications and build fast hardware for synchronous digital systems

REFERENCES

1. Keshab K. Parhi, " VLSI Digital Signal Processing Systems, Design andimplementation ", Wiley, Interscience, 2007.
2. U. Meyer – Baese, " Digital Signal Processing with Field Programmable GateArrays", Springer, 4th Edition, June 2014.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	1	
CO2	3		3	3	1	
CO3	3		3	3	1	
CO4	3		3	3	1	
CO5	3		3	3	1	

VL3103 HARDWARE DESCRIPTION LANGUAGES FOR RTL DESIGNS L T P C

3 0 4 5

UNIT I BASICS OF VHDL 6

Entity declaration - Architecture body - Creating I/O Ports for Different Data Types – Signal, Constant and variable - VHDL operators - Assignment operators, Logical operators, arithmetic operators and shift operators – Generic statement – VHDL statements - concurrent signal assignment statements and sequential statements – Packages, Components, Functions and Procedures – Test bench.

UNIT II BASICS OF VERILOG 6

Module – Module ports - Verilog operators – Data types – net, reg declarations - Constants and Arrays – Module parameters - Continuous and Procedural Assign statements – Conditional Expressions – Sequential statements - blocking and non-blocking assignments - Primitive instantiations – Module instantiations – Compiler directives – Test bench.

UNIT III HDL SYSTEM DESIGN 6

Combinational Circuit Design – Adder, Subtractor, Comparator, Priority encoder, Mux/Demux, Code converters, Array multiplier – Sequential circuit design – Latch, Flip flops, Registers, Shift registers, Counters, Sequential multiplier, State machine designs

UNIT IV DESIGN CONSIDERATIONS & VERIFICATION 6

Timing Parameters – Metastability – Positive and Negative Clock skew – Setup slack and Hold slack – Clock latency – Area, Speed and Power requirements, Testing and verification.

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UNIT V CASE STUDIES 6

A Pipelined Multiplier Accumulator – ALU Design – Single port and Dual port Memory design – Design of DSP modules and MAC unit – IP cores: creation and usage.

TOTAL:45 PERIODS

LAB EXPERIMENTS:

1. HDL realization and timing analysis of
   - Combinational circuits namely 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder.
   - Sequential circuits namely D-FF, Shift registers (SISO, SIPO, PISO, bidirectional), Synchronous Counters.
2. FPGA implementation of PCI Bus & arbiter.
3. Realization of UART/ USART implementation in HDL and design validation using test vector generation.
4. FPGA realization of single port SRAM and capturing the signal in DSO.
5. Back annotation and timing analysis of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
6. Realization of Discrete Fourier transform/Fast Fourier Transform algorithm in HDL and observing the spectrum in simulation.
7. Design and implement FIR and IIR filters
8. Design and implement adaptive filters

TOTAL: 60 PERIODS

COURSE OUTCOMES:

At the end of this course students will be able to

CO1: Use the basic data types and operators in Verilog / VHDL
CO2: Design arithmetic modules using Verilog and VHDL
CO3: Analyse power dissipation and propagation delay of the RTL modules
CO4: : Ability to Validate the design in FPGA starting from design entry to back annotation.
CO5: Design macro modules such as ALU, MAC, etc

REFERENCES:

1. Pong P. Chu, RTL Hardware Design using VHDL Coding for Efficiency, Portability, and Scalability, Wiley Interscience Publication, 2006, ISBN-13: 978-0-471-72092-8.
2. Ming Bo Lin, Digital System Designs and Practices – using Verilog HDLand FPGAs, Wiley India Pvt. Ltd., 2008, Reprint 2012.
3. Peter J.Ashenden, The Designer's Guide to VHDL, Third Edition, Elsevier, 2008. ISBN: 978-0-12-088785-9.
4. Peter J.Ashenden, Digital Design – An Embedded Systems Approach using Verilog, Elsevier Inc., 2008, ISBN: 978-0-12-369527-7.
5. Vaibbhav Taraate, ASIC Design and Synthesis – RTL Design using Verilog, Springer, 2021.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1			2	1	
CO2	2	2	2	2	1	

CO3	1			2	1	
CO4	3	3	3	3	1	
CO5	3	3	3	3	1	

VL3201 **DATA CONVERTERS IC DESIGN** **L T P C**
3 0 0 3

UNIT I INTRODUCTION & CHARACTERISTICS OF AD/DA CONVERTER CHARACTERISTICS **9**

Evolution, types and applications of AD/DA characteristics, issues in sampling, quantization and reconstruction, oversampling and antialiasing filters.

UNIT II SWITCH CAPACITOR CIRCUITS AND COMPARATORS **9**

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. offset cancellation, Op Amp offset cancellation, Calibration techniques

UNIT III NYQUIST RATE D/A CONVERTERS **9**

Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs, issues in current element matching, clock feed through, zero order hold circuits, DNL, INL and other performance metrics of ADCs and DACs

UNIT IV PIPELINE AND OTHER ADCs **9**

Performance metrics, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V SIGMA DELTA CONVERTERS **9**

STF, NTF, first order and second order sigma delta modulator characteristics, Estimating the maximum stable amplitude, CTDSMs, Opamp nonlinearities

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to carry out the design calculations for developing the various blocks associatedwith a typical CMOS AD or DA converter.
CO2: Ability to design and implement circuits using switched capacitor concepts
CO3: Ability to analyze and design D/A converters
CO4: Ability to design different types of A/Ds
CO5: Ability to analyze and design sigma delta converters

REFERENCES:

1. Shanthi Pavan, Richard Schreier, Gabor C. Temes , “Understanding Delta-Sigma Data Converters”, Willey –IEEE Press, 2nd Edition, 2017.
2. Behzad Razavi, “Principles of data conversion system design”, IEEE press, 1995.
3. M. Pelgrom, “Analog-to-Digital Conversion”, Springer, 4th Edition, January 2002.
4. Rudy van de Plassche, “CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters” Kluwer Acedamic Publishers, Boston, 2 nd Edition, December 2010.

5. J. G. Proakis, D. G. Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Prentice Hall, 4th Edition, January 2014.
6. VLSI Data Conversion Circuits EE658 recorded lectures available at http://www.ee.iitm.ac.in/~nagendra/videolecture

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	1	
CO2	3		3	3	1	
CO3	3		3	3	1	
CO4	3		3	3	1	
CO5	3		3	3	1	

VL3202 LOW POWER VLSI DESIGN L T P C

3 0 4 5

UNIT I POWER DISSIPATION IN CMOS 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation inCMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Gate level low power design – Architecture level low power design – VLSI subsystem design of adders, multipliers, PLL, lowpower design.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – Advanced techniques – Special techniques, Adiabatic techniques – Physical design, Floor planning, placement and routing.

UNIT IV POWER ESTIMATION 9

Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER 9

Synthesis for low power – Behavioral level transform –Algorithms for low power – software design for low power.

TOTAL: 45 PERIODS

LIST OF EXPERIMENTS:

1. CMOS inverter design and performance analysis
   - Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain. Calculate VIL, VIH, NMH, NML for the inverter.
   - Plot VTC for CMOS inverter with varying VDD.
   - Plot VTC for CMOS inverter with varying device ratio.

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- Redesign the inverter for symmetrical transient response and minimum propagation delay to for a given load capacitance. Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH,
- Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

2. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum

3. Use Layout editor.

- Draw layout of a minimum size inverter using transistor from CMOS process library. Use Metal 1 as interconnect line between inverters.
- Run DRC, LVS and RC extraction. Make sure there is no DRC error.
- Extract the netlist. Use extracted netlist and obtain t_{PHL} t_{PLH} for the inverter using Spice.
- Use a specific interconnect length and connect and connect three inverters in a chain. Extract the new netlist and obtain t_{PHL} and t_{PLH} of the middle inverter.
- Compare new values of delay times with corresponding values obtained in part 'c'.

4. Analog circuits case studies - Schematic entry to GDS II layout
5. Digital logics case studies - RTL Design entry to GDS II layout
6. Verification of power reduction techniques by clock gating, power gating and factorization.

TOTAL: 60 PERIODS

COURSE OUTCOMES:

CO1: Ability to find the power dissipation of MOS circuits
CO2: Design and analyse various MOS logic circuits
CO3: Apply low power techniques for low power dissipation
CO4: Able to estimate the power dissipation of ICs
CO5: Ability to develop algorithm to reduce power dissipation by software.

REFERENCES:

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, January 2009.
2. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
3. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer, October 2012.
4. Gary Yeap, "Practical low power digital VLSI design", Kluwer, October 2012.
5. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, September 2012.
6. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons,inc. 2001.
7. J.Rabaey, "Low Power Design Essentials (Integrated Circuits and Systems)", Springer, 2009.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	1	
CO2	3		3	3	1	

CO3	3		3	3	1	
CO4	3		3	3	1	
CO5	3		3	3	1	

VL3203 MULTI-CORE ARCHITECTURE AND ISA VERIFICATION L T P C
3 0 0 3

UNIT I INTRODUCTION TO COMPUTER ORGANISATION 9

Computer types – Functional units of a computer – Bus structures – Software – Processor clock – Performance equation – Pipelining and parallel processing – Compiler – Performance measurement – Multiprocessor and Multicomputer

UNIT II PROCESSOR 9

CPU core architecture – Logic design conventions – Datapath – Pipelining Datapath and control – Data and control hazards – Exceptions – Single core to Multi-core architectures – SIMD and MIMD systems - ARM cortex A53 and Intel core i7 pipelines – Qualcomm Snapdragon 888 SoC

UNIT III INSTRUCTION SET ARCHITECTURE 9

RISC-V Instructions – Base, Single and Double precision floating point, Atomic, Compute instructions – Instruction set representation, Parallel Program Design

UNIT IV MEMORY ORGANISATION 9

Memory hierarchy – Types of Memory – SRAM, DRAM, Flash memory, Disk – Cache memory – Cache hit and miss – Cache mapping – Direct mapping, Associative mapping and Set-associative mapping – DDR4 RAM

UNIT V ISA VERIFICATION 9

Decimal to floating point converter design, Floating point arithmetic modules design and verification, OP-Code generation for integer, floating point, atomic, compressed instructions set.

COURSE OUTCOMES:

At the end of this course students will be able to

CO1: Analyse the computer bus structures, clock and performance.
CO2: Ability to develop test cases for exception handling, data and control hazards.
CO3: Develop the code for conventional arithmetic and floating point modules
CO4: Analyse the memory for cache hit and miss.
CO5: Design and verify the floating point arithmetic modules

REFERENCES

1. David Patterson and John. L. Hennessy – Computer Organization and Design (The hardware/software interface RISC-V Edition) Elsevier, 2018.
2. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”,. Tata McGraw Hill, Fifth Edition, 2002
3. Peter S. Pacheco, —An Introduction to Parallel Programming, Morgan-Kauffman/Elsevier, 2011

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4. Andrew Waterman, Yunsup Lee, David Patterson, Krste Asanović, “The RISC-V Instruction Set Manual, Volume I: User-Level ISA Version 2.1”, Technical Report UCB/EECS-2016-118, EECS Department, University of California, Berkeley, May 31, 2016
5. Andrew Waterman, Yunsup Lee, Rimas Avižienis, David A. Patterson, and Krste Asanović, “The RISC-V Instruction Set Manual, Volume II: Privileged Architecture Version 1.9”, Technical Report UCB/EECS-2016-129, EECS Department, University of California, Berkeley, July 8, 2016

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1			2	1	
CO2	2		2	2	1	
CO3	1			2	1	
CO4	3		3	3	1	
CO5				2	1	

VL3211 PCB DESIGN AND ASSEMBLY LABORATORY L T P C
0 0 4 2

LIST OF EXPERIMENTS:

1. Schematic capture using EDA tool.
2. Prepare PCB design layout and generate Gerber files and other files formats.
3. Design and fabrication of single layer PCB using traditional method.
4. PTH and via drilling in PCB by manual and automated (Bantam tools) methods.
5. Mechanical registration and riveting of PTH and via.
6. Design and fabrication of double layer PCB using laser technology.
7. Design and fabrication of PCB using Bantam tools (milling process).
8. Design and fabrication of PCB using Voltera V-one machine.
9. Design and fabrication of PCB using Bot Factory – SV2 multilayer PCB printing.
10. SMD placing on PCB using pick and place machine.
11. PCB assembly of SMD using reflow soldering with temperature profiling of reflow oven.
12. PCB assembly of THD using manual and robotic soldering.
13. PCB assembly of THD using Wave soldering and its temperature profiling.
14. Design and fabricate PCB for AVR RISC based microcontroller development board.
15. Perform PCB assembly in the microcontroller development board.
16. Optical inspection and Verification of the microcontroller development board.
17. Conductive emission and Radiative emission test for PCB.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

CO1: Capability of using EDA tools
CO2: Ability to design a schematic diagram

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CO3: Ability to convert a schematic into layout
CO4: Implement routing in board/layout diagram
CO5: Ability to fabricate a PCB by different fabrication methods

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1				3	2	
CO2		1	2	2	3	
CO3			3		2	
CO4				3	2	
CO5			2		1	

AP3058 WIRELESS SENSOR NETWORKS L T P C
3 0 0 3

UNIT I OVERVIEW OF WIRELESS SENSOR NETWORKS 9

Challenges for Wireless Sensor Networks-Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- case study, Enabling Technologies for Wireless Sensor Networks.

UNIT II ARCHITECTURES 9

Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts. Physical Layer and Transceiver Design Considerations

UNIT III MAC AND ROUTING 9

MAC Protocols for Wireless Sensor Networks, IEEE 802.15.4, Zigbee, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy- Efficient Routing, Geographic Routing.

UNIT IV INFRASTRUCTURE ESTABLISHMENT 9

Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT V DATA MANAGEMENT AND SECURITY 9

Data management in WSN, Storage and indexing in sensor networks, Query processing in sensor, Data aggregation, Directed diffusion, Tiny aggregation, greedy aggregation, security in WSN, Case studies using simulation tools.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to design implement simple wireless network concepts
CO2: Ability to design, analyze implement different network architectures
CO3: Ability to implement MAC layer and routing protocols

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CO4: Ability to deal with timing and control issues in wireless sensor networks
CO5: Ability to analyze and design secured wireless sensor networks

REFERENCES

1. Ian F. Akyildiz, Mehmet Can Vuran, “Wireless Sensor Networks”, John Wiley, January 2018.
2. Yingshu Li, My T. Thai,Weili Wu, “Wireless Sensor Networks and Applications”,Springer, 2008.
3. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless SensorNetworks" , John Wiley, January 2011.
4. Feng Zhao & Leonidas J. Guibas, “Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
5. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-s Technology, Protocols, And Applications”, John Wiley,January 2010.
6. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.
7. Bhaskar Krishnamachari, “Networking Wireless Sensors”, Cambridge Press,2005.
8. Mohammad Ilyas And Imad Mahgaob, “Handbook Of Sensor Networks: CompactWireless And Wired Sensing Systems”, CRC Press, 2014.
9. Wayne Tomasi, “Introduction To Data Communication And Networking”, Pearson Education”, 2007.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			1	2		
CO2			2	2		
CO3	1		3	3	1	1
CO4	1		2	2		
CO5	1	1	2	3	1	1

VL3001 PCB CIRCUIT DESIGN L T P C
3 0 0 3

UNIT I BASICS OF PCB DESIGN, TOOLS & INDUSTRY STANDARDS 9

Printed Circuit Board Fabrication- PCB cores and layer stack-up. PCB fabrication process- Photolithography and chemical etching, Mechanical milling and Layer registration. Function of the Layout in the PCB Design Process. Design Files Created by Layout - Layout format files, Post process (Gerber) files, PCB assembly layers and files. Introduction to the Standards Organizations, Classes and Types of PCBs, Introduction to Standard Fabrication Allowances, PCB Dimensions and Tolerances, Copper Trace and Etching Tolerances, Standard Hole Dimensions, Solder mask Tolerance.

UNIT II PCB DESIGN FLOW USING CAD TOOL 9

Overview of Computer-Aided Design. Setting up the user account, Starting a new project, Schematic Entry, Placing and wiring (connecting) the parts, Converting Schematic to Layout, Layout Environment and Tool Set, Designing the PCB with Layout – Setting constraints, Placing the parts, Auto routing and the Manual routing, Performing a design rule check, Making a board outline, Post processing the board design for manufacturing, Submitting Gerber files and requesting a quote,

Annotating the layer types and stack-up, Receipt inspection and testing, Nonstandard Gerber files.

UNIT III DESIGN FOR MANUFACTURING 9

PCB Assembly and Soldering Processes- Component Placement and Orientation Guide, Component Spacing for Through-hole Devices (THDs). Component Spacing for Surface Mounted Devices (SMDs), Mixed THD and SMD Spacing Requirements. Footprint and Pad stack Design for PCB Manufacturability- Land Patterns for SMDs- Land Patterns for THDs, Pad stack design, Hole-to-lead ratio, PTH land dimension (annular ring width), Clearance between plane layers and PTHs Solder mask and solder paste dimensions.

UNIT IV PCB DESIGN FOR SIGNAL INTEGRITY 9

Signal Integrity Overview, Differential Traces and Impedance, Power Systems, Circuit Design Issues Not Related to PCB Layout, Issues Related to PCB Layout – surge, transient, crosstalk, ESD, Ground Planes and Ground Bounce, PCB Electrical Characteristics, PCB Routing Topics.

UNIT V EMERGING PCB FABRICATION PROCESSES 9

Additive manufacturing – Fundamentals, classification, advantages and standards. Stereo lithography (SL), Three Dimensional Printing - FDM, Materials and Applications, Voltera-V-one PCB double side Printer, Bot Factory- SV2-multi layer PCB printer, LPKF circuit board plotter and LDS Prototyping, Subtractive manufacturing – Laser technology (IPG and Raycus).

TOTAL : 45 PERIODS

COURSE OUTCOMES

CO1: Ability to apply the basics, industry standards related to the design of PCBs.
CO2: Ability to develop PCB design using software
CO3: Ability to design plated through-holes, surface-mount lands, and Layout footprints .
CO4: Ability to construct Capture parts using the Capture Library Manager and Part Editorand the PSpice Model Editor.
CO5: Ability to fabricate PCBs

REFERENCES:

1. Kraig Mitzner, Complete PCB Design Using OrCad Capture and Layout, Newness, 1st Edition, 2009.
2. Simon Monk, “Make Your Own PCBs with EAGLE: From Schematic Designs to Finished Boards”, McGraw-Hill Education TAB, 2nd Edition, 2017.
3. Douglas Brooks, “Signal Integrity Issues and Printed Circuit Board Design”, PrenticeHall PTR, 2012.
4. Lee W. Ritchey , John Zasio, Kella J. Knack, “ Right the First Time: a PracticalHandbook on High Speed Pcb and System Design”, Speeding Edge , 2003.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2					
CO2			3			
CO3			2			
CO4			2	3		
CO5		1	1	3	2	3

AP3051 ADVANCED MICROPROCESSORS AND MICROCONTROLLERS L T P C
3 0 0 3

UNIT I MICROPROCESSOR ARCHITECTURE 9

Instruction Set – Data formats –Addressing modes – Memory hierarchy –register file – Cache –Virtual memory and paging – Segmentation- pipelining –the instruction pipeline – pipeline hazards – instruction level parallelism – reduced instruction set –Computer principles – RISC versus CISC.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

CPU Architecture- Bus Operations – Pipelining – Brach predication – floating point unit- Operating Modes –Paging – Multitasking – Exception and Interrupts – Instruction set – addressing modes – Programming the Pentium processor.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE – ARM 9

Organization of CPU – Bus architecture –Memory management unit - ARM instruction set- Thumb Instruction set- addressing modes – Programming the ARM processor.

UNIT IV MSP430 16 - BIT MICROCONTROLLER 9

The MSP430 Architecture- CPU Registers - Instruction Set, On-Chip Peripherals - MSP430 - Development Tools, ADC - PWM - UART - Timer Interrupts - System design using MSP430Microcontroller.

UNIT V PIC MICROCONTROLLER 9

CPU Architecture – Instruction set – interrupts- Timers- I2C Interfacing –UART- A/D Converter –PWM and introduction to C-Compilers.

TOTAL:45 PERIODS

COURSE OUTCOMES:

CO1: Ability to learn the fundamentals of microprocessor architecture.
CO2: Ability to know and appreciate the high performance features in CISC architecture.
CO3: Ability to know and appreciate the high performance features in RISC architecture.
CO4: Ability to perceive the basic features in Motorola microcontrollers.
CO5: Ability to interpret and understand PIC Microcontroller.

REFERENCES:

1. Daniel Tabak , „" Advanced Microprocessors" McGraw Hill.Inc., 2nd Edition, November 2011.
2. James L. Antonakos , " The Pentium Microprocessor", Pearson Education , January 2002.
3. Steve Furber , " ARM System –On –Chip architecture", Addision Wesley , January 2014.
4. Gene .H.Miller ." Micro Computer Engineering ", Pearson Education , 2003.
5. John .B.Peatman , " Design with PIC Microcontroller" , Prentice hall, January 2002.
6. John H.Davis , "MSP 430 Micro controller basics", Elsevier, 2008.
7. James L.Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson Education 1999, Content Revision added Date 2020.
8. Barry.B.Breg, "The Intel Microprocessors Architecture, Programming and Interfacing " , PHI,2008.
9. Valvano "Embedded Microcomputer Systems", January 2012.
10. Readings: Web links -- www.ocw.mit.edu, www.arm.com

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Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1		1			
CO2	1			3	1	1
CO3	1		2	3	1	1
CO4	1		1	3	2	1
CO5	1		1	3	2	1

AP3052 ELECTRONICS FOR SOLAR POWER L T P C

3 0 0 3

UNIT I INTRODUCTION TO SOLAR POWER 9

Semiconductor – properties - energy levels - basic equations of semiconductor devices physics - Basic characteristics of sunlight - Solar angles - day length - angle of incidence on tilted surface – Sun path diagrams – Equivalent circuit of PV cell, PV cell characteristics (VI curve,PV curve) - Maximum power point, V_{MP}, I_{MP}, V_{OC}, I_{SC} – types of PV cell - Block diagram of solar photo voltaic system, PV array sizing.

UNIT II DC-DC CONVERTER 9

Principles of step-down and step-up converters – Analysis and design issues of buck, boost, buck-boost and Cuk converters – time ratio and current limit control – Case Study : Solar power based power system design with converters.

UNIT III MAXIMUM POWER POINT TRACKING 9

Direct Energy transmission, Impedance Matching, Maximum Power Point Tracking (MPPT) - Function of MPPT, P&O method, INC Method, Fractional Open circuit voltage method, Fractional short circuit current method, parasitic capacitance and other MPPT techniques, Development of hardware, algorithms using processors for Standalone and Grid tied systems.

UNIT IV BATTERY 9

Types of Battery, Battery Capacity – Units of Battery Capacity-impact of charging and discharging rate on battery capacity-Columbic efficiency-Voltage Efficiency, Charging – Charge Efficiency, Charging methods, State of Charge, Charging Rates, Discharging - Depth of discharge-Discharge Methods, selection of Battery and sizing, Case Study : Electric Vehicle Battery Management System (EV-BMS).

UNIT V SIMULATION OF PV MODULE & CONVERTERS 9

Matlab Simulation of PV module - VI Plot, PV Plot, finding VMP, IMP, Voc, Isc of PV module, Simulation of DC to DC converter -buck, boost, buck-boost and Cuk converters, standalone and grid tied photo voltaic system. FPGA based design and simulation of MPPT controllers**.**

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to analyze PV cells and power availability at a given location

CO2: Ability to design and realize dc-dc converters for solar power utilization

CO3: Ability to design algorithms for improving solar power utilization

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CO4: Ability to deal with battery issues and selection
CO5: Ability to design and simulate PV systems to validate its performance.

REFERENCES:

1. Chetan Singh Solanki, "Solar Photovoltaic: Fundamentals, Technologies and Applications",PHI Ltd., 3 rd Edition, January 2015.
2. Tommarkvart, Luis castaner, "Solar cells; materials, manufacture and operation", Elsevier, 2005.
3. G.D .Rai, "Solar energy utilization ", Khanna publishes, January 1995.
4. Ned Mohan, Undeland and Robbin, "Power Electronics: converters, Application andDesign", John Wiley and sons.Inc, Newyork, 3rd Edition, March 2002.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1			2	3	3
CO2	2	1	2	2	3	3
CO3	1			2	3	3
CO4	3	1	3	3	3	3
CO5				2	3	3

AP3056 ROBOTICS AND INTELLIGENT SYSTEMS L T P C
3 0 0 3

UNIT I INTRODUCTION: 9

Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution,accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.

UNIT II ROBOT GRIPPERS: 9

Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots:- Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.

UNIT III DRIVES AND CONTROL SYSTEMS: 9

Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems -Types of Controllers, Introduction to closed loop control .Control Technologies in Automation:- Industrial Control Systems, Process Industries Verses Discrete-Manufacturing Industries, Continuous Verses Discrete Control, Computer Process and its Forms. Control System Components such as Sensors, Actuators and others.

UNIT IV MACHINE VISION SYSTEM 9

Vision System Devices, Robot Programming:- Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands,

subroutines, Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.

UNIT V MODELING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION 9

Introduction, need for system Modeling, Building Mathematical Model of a manufacturing Plant, Modern Tools- Artificial neural networks in manufacturing automation, AI in manufacturing, Fuzzy decision and control, robots and application of robots for automation. Artificial Intelligence:- Introduction to Artificial Intelligence, AI techniques, Need and application of AI. Other Topics in Robotics:- Socio-Economic aspect of robotisation. Economical aspects for robotdesign, Safety for robot and associated mass, New Trends & recent updates in robotics.

TOTAL:45 PERIODS

COURSE OUTCOMES:

CO1: Ability to implement simple concepts associated with Robotics and Automation
CO2: Ability to use various Robotic sub-systems
CO3: Ability to use kinematics and dynamics to design exact working pattern of robots
CO4: Ability to implement computer vision algorithms for robots
CO5: Be aware of the associated recent updates in Robotics

REFERENCES:

1. John J. Craig, "Introduction to Robotics (Mechanics and Control)", Addison-Wesley, 4th Edition, February 2017.
2. Mikell P. Groover et. Al., "Industrial Robotics: Technology, Programming and Applications, McGraw – Hill International", 2nd Edition 2017.
3. Shimon Y. Nof , "Handbook of Industrial Robotics" , John Wiley Co, 2nd Edition, January 2013.
4. Automation, "Production Systems and Computer Integrated Manufacturing", M.P. Groover, Pearson Education, 4th Edition, July 2016.
5. W.P. David, "Industrial Automation", John Wiley and Sons. February 2011.
6. Richard D. Klafter , Thomas A. Chemielewski, Michael Negin, "Robotic Engineering : An Integrated Approach" , Prentice Hall India, 2002.
7. R.C. Dorf, "Handbook of design, manufacturing & Automation", John Wiley and Sons, November 1994.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1		2	2	2	
CO2			2	3		
CO3	1		1			
CO4	1		2	1		
CO5			2			

VL3002	RF SYSTEM DESIGN	L T P C 3 0 0 3

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES 9

Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct upconversion Transmitter, Two step upconversion Transmitter.

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS 9

S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIER 9

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations

UNIT IV MIXERS AND OSCILLATOR 9

Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.

UNIT V PLL AND FREQUENCY SYNTHESIZERS 9

Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to explore user specifications for RF systems
CO2: Ability to analyze and design RF amplifiers
CO3: Ability to analyze and design RF power amplifiers
CO4: Ability to analyze and design RF mixers and oscillators
CO5: Ability to design PLL for RF applications

REFERENCES:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 2nd Edition, January 2013.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, January 2015.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2nd Edition, November 2017.
5. Recorded lectures and notes available at . http://www.ee.iitm.ac.in/~ani/ee6240/

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Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	1	2	2
CO2	3		3	1	2	2
CO3	3		3	1	2	2
CO4	3		3	1	2	2
CO5	3		3	1	2	2

AP3057 SIGNAL INTEGRITY FOR HIGH SPEED DESIGN L T P C
3 0 0 3

UNIT I SIGNAL PROPAGATION ON TRANSMISSION LINES 9

Transmission line equations, wave solution, wave *vs*. circuits, initial wave, delay time, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters, PCB layer stackups and layer/Cu thicknesses, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline Reflection and terminations for logic gates, fan-out,logic switching , input impedance into a transmission-line section, reflection coefficient, skin- effect, dispersion.

UNIT II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far- end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNIT III NON-IDEAL EFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance , Transmission line losses – Rs, tanδ , routing parasitic, Common-mode current, differential-mode current , Connectors.

UNIT IV POWER CONSIDERATIONS AND SYSTEM DESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams , jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNIT V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to identify sources affecting the speed of digital circuits.
CO2: Ability to identify methods to improve the signal transmission characteristics
CO3: Ability to analyze non-ideal effects
CO4: Ability to analyze system power dissipation
CO5: Ability to analyze clocking strategies

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REFERENCES

1. H. W. Johnson and M. Graham, High-Speed Digital Design: A Handbook of Black Magic, Prentice Hall, January 2003.
2. Douglas Brooks, Signal Integrity Issues and Printed Circuit Board Design, Prentice HallPTR , November 2012.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, January 2014.
4. Eric Bogatin , Signal Integrity – Simplified , Prentice Hall PTR, 3rd Edition, June 2018.

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICE from synopsis, www.synopsys.com/products/ mixedsignal/hspice/hspice.html
3. SPECCTRAQUEST from Cadence, http://www.specctraquest.com

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3			1
CO2	2		3		1	
CO3	2		3		1	
CO4	2		3		1	
CO5	2		3		1	

AP3053 EMI AND EMC IN SYSTEM DESIGN L T P C
3 0 0 3

UNIT I EMI/EMC CONCEPTS 9

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES 9

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS 9

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations

UNIT V EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

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TOTAL:45 PERIODS

COURSE OUTCOMES:

CO1: Ability to gain knowledge to understand the concept of EMI / EMC related to productdesign & development.

CO2: Ability to analyze the different EM coupling principles and its impact on performance of electronic system.

CO3: Ability to analyze electromagnetic interference, highlighting the concepts of both susceptibility andimmunity

CO4: Ability to interpret various EM compatibility issues with regard to the design of PCBs and ways toimprove the overall system performance

CO5: Ability to obtain broad knowledge of various EM radiation measurement techniques and the present leading edge industry standards in different countries

REFERENCES:

1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, Newyork, 1996.
2. Henry W.Ott.,”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, Artech house, Norwood, 3rd Edition, 1987.
4. C.R.Paul,”Introduction to Electromagnetic Compatibility” , John Wiley and Sons, Inc, 2 nd Edition, January 2010.
5. Don R.J.White Consultant Incorporate, “Handbook of EMI/EMC”, Vol I-V, 1988.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2			
CO2	1				3	3
CO3			2			
CO4			2	3	2	3
CO5					3	2

VL3003 HARDWARE AND SOFTWARE CO-DESIGN L T P C

3 0 0 3

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous implementation - Processor Synthesis, Single- Processor Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi-Processor Architectures, Comparison of Co-Design approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture, Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures andApplication System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems, Mixed Systems and Less Specialized Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to describe the broad range of system architectures and design methodologies that currently exist and define their fundamental attributes.

CO2: Ability to discuss the dataflow models as a state-of-the-art methodology to solve co-design problems and to optimize the balance between software and hardware.

CO3: Ability to understand in translating between software and hardware descriptions through co-design methodologies.

CO4: Ability to analyse the state-of-the-art practices in developing co-design solutions to problems using modern hardware/software tools for building prototypes.

CO5: Ability to apply the concurrent specification from an algorithm, analyze its behavior and partition the specification into software (C code) and hardware (HDL) components

REFERENCES:

1. Patrick Schaumont, “A Practical Introduction to Hardware / Software Code sign”, Springer, 2nd Edition, December 2014.
2. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated EmbeddedSystems”, Kluwer Academic Publisher, December 2010.
3. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Publisher, January 2007.
4. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design”, Kaufmann Publisher,2001.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	1	
CO2	3		3	3	1	
CO3	3		3	3	1	
CO4	3		3	3	1	
CO5	3		3	3	1	

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VL3004 RECONFIGURABLE COMPUTING L T P C
3 0 0 3

UNIT I RECONFIGURABLE COMPUTING HARDWARE 9

Domain specific processors, Application specific processors, Reconfigurable Computing Systems, Evolution of reconfigurable systems, Characteristics of RCS, advantages and issues. Device Architecture, Reconfigurable Computing Architectures, Reconfigurable Computing Systems, Reconfiguration Management

UNIT II PROGRAMMING RECONFIGURABLE SYSTEMS 9

Compute Models and System Architectures, Programming FPGA Applications in Verilog HDL, Compiling C for Spatial Computing, Programming Streaming FPGA Applications Using Block Diagrams in Simulink, Programming Data Parallel FPGA Applications, Operating System Support for Reconfigurable Computing, The JHDL Design and Debug System

UNIT III MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

Technology Mapping, Placement for General-purpose FPGAs, Datapath Composition, Specifying Circuit Layout on FPGAs, PathFinder: A Negotiation-based, Performance-driven Router for FPGAs, Retiming, Repipelining, and C-slow Retiming, Configuration Bitstream Generation, Fast Compilation Techniques

UNIT IV APPLICATION DEVELOPMENT 9

Implementing Applications with FPGAs, Instance-specific Design, Precision Analysis for Fixed- point Computation, Distributed Arithmetic, CORDIC Architectures for FPGA Computing, Hardware/Software Partitioning

UNIT V CASE STUDIES OF FPGA APPLICATIONS 9

SPIHT Image Compression, Automatic Target Recognition Systems on Reconfigurable Devices, Multi-FPGA Systems: Logic Emulation, The Implications of Floating Point for FPGAs, Evolvable FPGAs, Network Packet Processing in Reconfigurable Hardware, Active Pages:Memory-centric Computation

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to apply the fundamentals of the reconfigurable computing and reconfigurable architectures.

CO2: Ability to articulate the design issues involved in reconfigurable computing systems with a specific focus on Field Programmable Gate Arrays (FPGAs) both in theoretical and application levels.

CO3: Ability to develop the performance trade-offs involved in designing a reconfigurable computing platform with a specific focus on the architecture of a configurable logic block and the programmable interconnect.

CO4: Ability to explore the state of the art reconfigurable computing architectures spanning fine grained (look up table based processing elements) to coarse grained (arithmetic logic unit level processing elements) architectures.

CO5: Ability to design the architect reconfigurable systems and utilize them for solving challenging computational problems.

REFERENCES:

1. Scott Hauck and Andre` DeHon, “Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation”, Morgan Kaufmann, July 2010.
2. Stephen M. Trimberger, “Field – programmable Gate Array Technology”, Springer, 2007.
3. CliveMaxfield, “The Design Warrior’s Guide to FPGAs: Devices, Tools and Flows”, Newnes, Elsevier, 2006.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	1	
CO2	3		3	3	1	
CO3	3		3	3	1	
CO4	3		3	3	1	
CO5	3		3	3	1	

VL3005 EVOLVABLE HARDWARE L T P C
3 0 0 3

UNIT I INTRODUCTION 9

Traditional hardware systems and its Limitations, Evolvable hardware, Characteristics of evolvable circuits and systems, Technology-Extrinsic and intrinsic evolution Offline and online evolution, Applications and scope of EHW

UNIT II EVOLUTIONARY COMPUTATION 9

Fundamentals of Evolutionary algorithms, Components of EA, Variants of EA, Genetic algorithms, Genetic Programming, Evolutionary strategies, Evolutionary programming, Implementations – Evolutionary design and optimizations, EHW – Current problems and potential solutions

UNIT III RECONFIGURABLE DIGITAL DEVICES 9

Basic architectures – Programmable Logic Devices, Field Programmable Gate Arrays (FPGAs), Using reconfigurable hardware – Design phase, Execution phase, Evolution of digital circuits

UNIT IV RECONFIGURABLE ANALOG DEVICES 9

Basic architectures – Field Programmable Transistor arrays (FPTAs), Analog arrays, MWMs,Using reconfigurable hardware – Design phase, Execution phase, Evolution of analog circuits

UNIT V APPLICATIONS OF EHW 9

Synthesis vs. adaptation, Designing self-adaptive systems, Fault-tolerant systems, Real-time systems, intrinsic reconfiguration for online systems, EHW based fault recovery and future work

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to know the fundamentals of computational models and computers which have appeared at the intersection of hardware and artificial intelligence to solve hard computational problems.

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CO2: Ability to develop the principles of bio-inspired and unconventional computational systems.
CO3:Ability to explore the reconfigurable digital architectures and its computational intelligence techniques.
CO4:Ability to explore the reconfigurable analog architectures and its computational intelligence techniques.
CO5:Ability to explore the typical applications of bio-inspired and other unconventional techniques in the phase of design, implementation and runtime of a computational device.

REFERENCES:

1. Garrison W. Greenwood and Andrew M. Tyhrrell, “Introduction to Evolvable Hardware: A Practical Guide for Designing Self- Adaptive Systems”, Wiley-IEEE Press, 2006.
2. Tetsuya Higuchi, Xin Yao and Yong Liu, “Evolvable Hardware”, Springer-Verlag, 2004.
3. Lukas Sekanina, “Evolvable Components: From Theory to Hardware Implementations”, Springer, 2004.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	1	
CO2	3		3	3	1	
CO3	3		3	3	1	
CO4	3		3	3	1	
CO5	3		3	3	1	

VL3006 POWER MANAGEMENT AND CLOCK DISTRIBUTION CIRCUITS L T P C
3 0 0 3

UNIT I VOLTAGE AND CURRENT REFERENCES 9

Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent Biasing, Temperature Independent Biasing, PTAT Current Generation, Constant Gm Biasing

UNIT II LOW DROP OUT REGULATORS 9

Analog Building Blocks, Negative Feedback, Performance Metrics, AC Design, Stability, Internal and External Compensation, PSRR – Internal and External compensation circuits.

UNIT III OSCILLATOR FUNDAMENTALS 9

General considerations, Ring oscillators, LC oscillators, Colpitts Oscillator, Jitter and Phase noise in Ring Oscillators, Impulse Sensitivity Function for LC & Ring Oscillators, Phase Noise inDifferential LC Oscillators.

UNIT IV CLOCK DISTRIBUTION CIRCUITS 9

PLL Fundamental, PLL stability, Noise Performance, Charge-Pump PLL Topology, CPPLLBuilding blocks, Jitter and Phase Noise performance, DLL fundamentals.

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UNIT V CLOCK AND DATA RECOVERY CIRCUITS 9

CDR Architectures, Trans Impedance Amplifiers and Limiters, CMOS Interface, Linear Half Rate CMOS CDR Circuits, Wide capture Range CDR Circuits.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to design Band gap reference circuits and Low Drop Out regulator for a given specification.

CO2: Ability to design specification related to Supply and Clock generation circuits

CO3: Ability to choose oscillator topology and design meeting the requirement of clock generation circuits.

CO4: Ability to design clock generation circuits in the context of high speed I/Os, High speed Broad Band Communication circuits.

CO5: Ability to design Data Conversion Circuits

REFERENCES:

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order band gap circuits", John wiley& Sons Inc, 2002.
2. Gabriel.A. Rincon-Mora, "Analog IC Design With Low-Dropout Regulators", McGraw-HillProfessional Pub, 2 nd Edition, May 2014.
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2 nd Edition, November 2017.
4. Floyd M. Gardner ,"Phase Lock Techniques" John wiley& Sons, Inc 2005.
5. Michiel Steyaert, Arthur H.M. van Roermund, Herman Casier, "Analog Circuit Design: High Speed Clock and Data Recovery, High-performance Amplifiers Power Management", springer, November 2010.
6. BehzadRazavi, "Design of Integrated circuits for Optical Communications", McGraw Hill, 2 nd Edition, October 2012.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2			
CO2			2			
CO3	2		2	3	1	
CO4			3		2	
CO5				2		

VL3007 TESTING OF VLSI CIRCUITS L T P C
3 0 0 3

UNIT I INTRODUCTION TO TESTING 9

Introduction – VLSI Testing Process and Test Equipment – Challenges in VLSI Testing - Test Economics and Product Quality – Fault Modeling – Relationship among Fault Models.

UNIT II LOGIC & FAULT SIMULATION & TESTABILITY MEASURES 9

Simulation for Design Verification and Test Evaluation – Modeling Circuits for Simulation – Algorithms for True Value and Fault Simulation – SCOAP Controllability and Observability.

UNIT III TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS **9**

Algorithms and Representations – Redundancy Identification – Combinational ATPG Algorithms – Sequential ATPG Algorithms – Simulation Based ATPG – Genetic Algorithm Based ATPG.

UNIT IV DESIGN FOR TESTABILITY **9**

Design for Testability Basics – Testability Analysis - Scan Cell Designs – Scan Architecture –Built-In Self-Test – Random Logic BIST – DFT for other Test Objectives.

UNIT V FAULT DIAGNOSIS **9**

Introduction and Basic Definitions – Fault Models for Diagnosis – Generation for Vectors for Diagnosis – Combinational Logic Diagnosis - Scan Chain Diagnosis – Logic BIST Diagnosis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to find VLSI Testing Process.
CO2: Ability to develop Logic Simulation and Fault Simulation.
CO3: Ability to develop Test for Combinational and Sequential circuits.
CO4: Ability to apply the Design for Testability.
CO5: Ability to perform Fault Diagnosis.

REFERENCES:

1. Laung-Terng Wang, Cheng-Wen Wu and Xiaoqing Wen, “VLSI Test Principles and Architectures”, Elsevier, 2017.
2. Michael L. Bushnell and Vishwani D. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits” , Kluwer Academic Publishers, 2017.
3. Niraj K. Jha and Sandeep Gupta, “Testing of Digital Systems”, Cambridge University Press, 2017.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2			
CO2			2			
CO3	2		2	3	1	
CO4			3		2	
CO5				2		

VL3008 SoC DESIGN **L T P C**
3 0 0 3

UNIT I ASIC **9**

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SoC , architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

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UNIT II NISC **9**

NISC Control Words methodology, NISC Applications & Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT III SIMULATION **9**

Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT IV LOW POWER SOC DESIGN / DIGITAL SYSTEM **9**

Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT V SYNTHESIS **9**

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to identify & formulate a given problem in framework of SoC
CO2: Ability to develop NISC Architecture, ADL and ASIP
CO3: Ability to simulate SoC at various levels.
CO4: Ability to design low power SoC / Digital System
CO5: Ability to map the resources and optimize the system performance

REFERENCES:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006.
3. RochitRajsuman, “System-on- a-chip: Design and test”, Advantest America R & DCenter, 2000.
4. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008.
5. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”, Wiley, 2011.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	1	
CO2	3		3	3	1	
CO3	3		3	3	1	

CO4	3		3	3	1	
CO5	3		3	3	1	

VL3051 **ASIC DESIGN** **L T P C**

3 0 0 3

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN **9**

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS WITH LOGIC CELLS AND I/O CELLS **9**

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECUTRE **9**

Architecture and configuration of Artix / Cyclone and Kintex Ultra Scale / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING **9**

Logic synthesis - Floor Planning Goals and Objectives, Measurement of Delay in floor planning,Floor planning tools ,I/O and Power planning, Clock planning, Placement Algorithms. Routing: Global routing, Detailed routing, Special routing.

UNIT V SYSTEM-ON-CHIP DESIGN **9**

SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High performance filters using delta-sigma modulators.
Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to apply logical effort technique for predicting delay, delay minimization and FPGA architectures.
CO2: Ability to design logic cells and I/O cells.
CO3: Ability to analyze the various resources of recent FPGAs.
CO4: Ability to use algorithms for floor planning and placement of cells and to apply routing algorithms for optimization of length and speed.
CO5: Ability to analyze high performance algorithms available for ASICs.

REFERENCES:

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson, 2003.
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science, August 2007.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2nd Edition, April 2017.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw Hill, 1994.

5. Douglas J. Smith, “HDL Chip Design”, Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994
7. S.Pasricha and N.Dutt, “On-Chip Communication Architectures System on Chip Interconnect”, Elsevier, 2008.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1			2	1	
CO2	2		2	2	1	
CO3	1			2	1	
CO4	3		3	3	1	
CO5		1		2	1	

VL3009 CAD FOR VLSI CIRCUITS L T P C

3 0 0 3

UNIT I INTRODUCTION 9

Introduction to VLSI Design Methodologies – VLSI Design Cycle – New Trends in VLSI DesignCycle – Physical Design Cycle – New Trends in Physical Design Cycle – Design Styles –Review of VLSI Design Automation Tools.

UNIT II DATA STRUCTURES AND BASIC ALGORITHMS 9

Introduction to Data Structures and Algorithms – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable Problems – General Purpose Methods for Combinatorial Optimization.

UNIT III ALGORITHMS FOR PARTITIONING AND PLACEMENT 9

Layout Compaction – Problem Formulation – Algorithms for Constraint Graph Compaction – Partitioning – Placement – Placement Algorithms.

UNIT IV ALGORITHMS FOR FLOORPLANNING AND ROUTING 9

Floorplanning – Problem Formulation – Floorplanning Algorithms – Routing – Area Routing –Global Routing – Detailed Routing.

UNIT V MODELLING, SIMULATION AND SYNTHESIS 9

Simulation – Gate Level Modeling and Simulation – Logic Synthesis and Verification – Binary Decision Diagrams – High Level Synthesis.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to use various VLSI Design Methodologies and Design Methods.
CO2: Ability to apply different Data Structures and Algorithms for VLSI Design.
CO3: Ability to develop Algorithms for Partitioning and Placement.
CO4: Ability to develop Algorithms for Floorplanning and Routing.
CO5: Ability to design Algorithms for Modelling, Simulation and Synthesis.

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REFERENCES:

1. Sabih H. Gerez, “Algorithms for VLSI Design Automation”, Second Edition, Wiley-India, 2017.
2. Naveed A. Sherwani, “Algorithms for VLSI Physical Design Automation”, 3rd Edition, Springer, 2017.
3. Charles J. Alpert, Dinesh P. Mehta and Sachin S Sapatnekar, “Handbook of Algorithms forPhysical Design Automation, CRC Press, 1st Edition, 2

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2			
CO2			2			
CO3	2		2	3	1	
CO4			3		2	
CO5				2		

VL3010 ADVANCED SIGNAL PROCESSING L T P C
3 0 0 3

UNIT I INTRODUCTION TO RANDOM SIGNAL PROCESSING 9

Discrete Random Processes- Ensemble Averages, Stationary processes, Bias and Estimation, Auto-covariance, Autocorrelation, Parseval"s theorem, Wiener-Khintchine relation, White noise, Power Spectral Density, Spectral factorization, Filtering Random Processes.

UNIT II SIGNAL MODELING 9

ARMA (p,q) , AR (p), MA (q) models, Forward Linear Prediction, Backward Linear Prediction :Yule-Walker Method, Solution to Prony’s normal equation, Levinson Durbin Algorithm.

UNIT III SPECTRAL ESTIMATION 9

Estimation of spectra from finite duration signals, Nonparametric methods - Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric method, AR (p) spectral estimation and detection of Harmonic signals.

UNIT IV LINEAR ESTIMATION 9

Linear Minimum Mean-Square Error (LMMSE) Filtering: Wiener Hopf Equation, FIR Wiener filter, Noise Cancellation, Causal IIR Wiener filter, Noncausal IIR Wiener filter.

UNIT V ADAPTIVE FILTERS 9

FIR adaptive filters — adaptive filter based on steepest descent method- Widrow-Hopf LMS algorithm, Normalized LMS algorithm, Adaptive channel equalization, Adaptive echo cancellation, Adaptive noise cancellation, RLS adaptive algorithm.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to analyze discrete time random processes
CO2: Ability to obtain models for prediction and Estimation
CO3: Ability to analyze non-parametric methods and parametric methods for spectral estimation

CO4: Ability to design different MMSE filters
CO5: Ability to design adaptive filters for different applications.

REFERENCES:

1. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons, Inc, Singapore, 2002.
2. Dimitris G. Manolakis and Vinay K .Ingle ,“Applied Digital Signal Processing”, Cambridge University Press, 2011.
3. Fundamentals of Statistical Signal Processing: Estimation Theory(Vol 1), Detection Theory (Vol 2), .M. Kay's, Prentice Hall Signal Processing Series, 1993.
4. Linear Estimation, Kailath, Sayed and Hassibi, Prentice Hall Information and SciencesSeries, 1st Edition, 2000.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2	1		
CO2	3		2	1		
CO3	3		3	1		
CO4	3		3	2	1	1
CO5	3		3	2	1	1

AP3251 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modelling- State diagram, state table, state table assignment and reduction-Design of synchronous sequential circuits design of iterative circuits-ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – flow table reduction-races-state assignment- transition table and problems in transition table- design of asynchronous sequential circuit- Static, dynamic and essential hazards – mixed operating mode asynchronous circuits – designing vending machine controller

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method-path sensitization method – Boolean difference method - D algorithm – Kohavi algorithm – Tolerance techniques – The compact algorithm – Fault in PLA – Test generation-DFT schemes – Built in self test

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming logic device families – Designing a synchronous sequential circuit using PLA/PAL

– Designing ROM with PLA – Realization of finite state machine using PLD – FPGA – Xilinx FPGA- Xilinx 4000

UNIT V SYSTEM DESIGN USING VERILOG 9

Hardware Modelling with Verilog HDL – Logic System, Data Types and Operators For Modelling in Verilog HDL - Behavioral Descriptions in Verilog HDL – HDL Based Synthesis –Synthesis of Finite State Machines– structural modelling – compilation and simulation of Verilog code –Test bench - Realization of combinational and sequential circuits using Verilog – Registers – counters – sequential machine – serial adder – Multiplier- Divider – Design ofsimple microprocessor

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to analyse and design synchronous sequential circuits
CO2: Ability to analyse hazards and design asynchronous sequential circuits
CO3; Ability to apply the testing procedure for combinational circuits and PLA
CO4: Ability to design PLD and ROM
CO5: Ability to design and use programming tools for implementing digital circuits

REFERENCES:

1. Charles H.Roth Jr, “Fundamentals of Logic Design” Thomson Learning 5th Edition, October 2005.
2. M.D.Ciletti , Modeling, Synthesis and Rapid Prototyping with the Verilog HDL,Prentice Hall, 1999
3. M.G.Arnold, Verilog Digital – Computer Design, Prentice Hall (PTR),January 2009.
4. Nripendra N Biswas “Logic Design Theory” Prentice Hall of India,2001
5. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications,2002
6. Parag K.Lala “Digital system Design using PLD” B S Publications,2003
7. S. Palnitkar, Verilog HDL – A Guide to Digital Design and Synthesis, Pearson , 2003.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2			
CO2			2			
CO3	2		2	3	1	
CO4			3		2	
CO5				2		

VL3052 FUNDAMENTALS OF SPINTRONICS AND QUANTUM COMPUTING L T P C
3 0 0 3

UNIT I LAWS OF SPINTRONICS AND SPIN ORBIT 9

The Early History of Spin, Quantum Mechanics of Spin, Spin – Orbit interaction, Spin – Orbit interaction of Solids.

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UNIT II SPIN ELECTRON TRANSPORT 9

Basic Electron Transport, Basic Electron Transport in thin film, Conduction in Discontinuous film, Magneto-resistance, Spin-Dependent Scattering, Giant Magneto Resistance, Spin Dependent Tunneling, Tunnel Magneto-resistance, MTJ, STT, SOT.

UNITIII SPIN TRANSISTOR 9

Silicon based spin electron device, Spin field effect transistor Spin injection, spin diffusion, Spin LED: Fundamental and Application, Spin photo electronics Devices

UNIT IV ELECTRON SPINS IN QUANTUM DOTS AS QUBITS 9

Conventional Vs Quantum Computing - Quantum Communication - Requirements for Quantum Computing - Coupled Quantum Dots as Quantum Gates - Single-Spin Rotations - Read-Out of a Single Spin

UNIT V QUANTUM COMPUTING WITH SPINS 9

The quantum inverter - NAND without energy dissipation - Universal reversible gate: Toffoli-Fredkin gate, A-matrix – Quantum gate, Superposition states – Quantum parallelism - Universal quantum gates

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of this course students will be able to

CO1: Ability to learn the laws of spintronics and spin orbit.
CO2: Ability to obtain spin based transport and its characteristics.
CO3: Identify the types of spintronics based devices.
CO4: Design quantum gates using qubits.
CO5: Apply the quantum principles to quantum universal gates.

REFERENCES:

1. Bandyopadhyay S, Cahay M. Introduction to spintronics. CRC press; 2015.
2. Awschalom DD, Loss D, Samarth N, editors. Semiconductor spintronics and quantum computation. Springer Science & Business Media; 2013.
3. Hedin ER, Joe YS, editors. Spintronics in nanoscale devices. CRC Press; 2013 Aug 20.
4. D. J. Sellmyer, R. Skomski. Advanced Magnetic Nanostructures. SpringerPublishers, 2005.
5. S. Maekawa. Concepts in Spin Electronics. Oxford University Press; 2006.
6. D.D. Awschalom, R.A. Buhrman, J.M. Daughton, S.V. Molnar, and M.L. Roukes, Spin Electronics, Kluwer Academic Publishers, 2004.
7. Y.B. Xu and S.M.Thompson. Spin Materials and Technology. Taylor & Francis, 2006.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	2	1	
CO2	3		3	3	1	
CO3	3		3	3	1	
CO4	3		3	3	1	
CO5	3		3	3	1	

VL3055	NEUROMORPHIC COMPUTING	L T P C 3 0 0 3

UNIT I INTRODUCTION TO NEUROMORPHIC ENGINEERING 9

Introduction to neuromorphic engineering, Non-von Neumann computing approach, Neuron, Synapse, Synaptic plasticity rules, spike-time-dependent plasticity, Signaling and operation of Biological neurons, Neuron models- LIF, IF, HH

UNIT II SENSORY SYSTEMS AND LEARNING 9

Silicon retina, silicon cochlea, electronic nose, learning in silicon – supervised and unsupervised learning, Hebbian learning in silicon and cognitive functions in silicon – recognition, attention, artificial consciousness, Hybrid Neuron-Silicon system - Hodgkin-Huxley Model , Volterra-Poisson Model.

UNIT III NEUROMORPHIC COMPUTING 9

Spiking Neural Networks , Advanced Nanodevices for Neuron Implementation, Synaptic emulation - non-volatile memory, Flash, RRAM, Electro-chemical RAM, memristors, CNT, Interconnection Networks; Interconnection schemes for large non-spiking and spiking neural networks. ECRAMs.

UNIT IV NEUROMORPHIC HARDWARE IMPLEMENTATION 9

Hardware Implementation: Electronic synapses, Hardware Implementation of Neuron circuits, Hardware Implementation of Synaptic and Learning circuits, and System Design: Analysis of digital neuromorphic system design, architecture and performance characteristics of demonstrated chips employing digital neuromorphic VLSI, electronic synapses and other neuromorphic systems

UNIT V NETWORK DESIGN 9

Network Design, Network design example for visual application, auditory application, full system level power/energy dissipation considerations

TOTAL: 45 PERIODS

COURSE OUTCOME:

CO1: Ability to learn how electronics circuits mimic biological neurons
CO2 Ability to implement learning techniques and cognitive functions in Silicon
CO3 : Ability to build power-saving hardware building blocks for neuromorphic systems
CO4 : Ability to design and develop neuromorphic circuits
CO5: Ability to implement commercial neuromorphic system design for various real-world applications

REFERENCES:

1. Eric Kandel, James Schwartz, Thomas Jessell, Steven Siegelbaum, A.J. Hudspeth, Principles of neural science, McGraw Hill 2012, ISBN 0071390111
2. Dale Purves, Neuroscience, Sinauer, 2008, ISBN 0878936971
3. Shih-Chii Liu, Jörg Kramer, Giacomo Indiveri, Tobias Delbrück, Rodney Douglas, Analog VLSI: circuits and principles, MIT press, 2002, ISBN 0262122553
4. Carver Mead, Analog VLSI and neural systems, Addison-Wesley, 1989, ISBN0201059924
5. Kozma, R., (2012), Advances in Neuromorphic Memristor Science, Springer
6. Review papers on Neuromorphic Computing.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	3	2	
CO2	2		3	3	2	
CO3	2		3	3	2	
CO4	2		3	3	2	
CO5	2		3	3	2	

VL3053 MACHINE LEARNING IN VLSI DESIGN L T P C
3 0 0 3

UNIT I INTRODUCTION TO MACHINE LEARNING ARCHITECTURE 9

Artificial Neural Networks – Artificial Neuron and its mathematical model, Activation functions, Biases and threshold, Linear separability, Neural network architecture: single layer and multilayer feed forward networks, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning, Architecture for Multiply and Accumulate unit, Special function unit for Sigmoid and ReLu activation functions.

UNIT II SUPERVISED LEARNING AND UNSUPERVISED LEARNING 9

Multilayer Perceptron - Back propagation learning algorithm, Radial-basis function Networks Kernels and Support vector machines, Unsupervised learning - K Nearest Neighbors , Self-organizing Feature Maps, Gaussian Mixture Models.

UNIT III DEEP NEURAL NETWORKS 9

Convolutional Neural basics: kernels, padding, stride, channels, activation maps, Convolutional neural network: pooling, receptive field, batch normalization, Standard CNN architectures: LeNet, AlexNet, VGG, Inception, ResNet, GoogleNet, DenseNet; Performance comparison of different CNN architectures.

UNIT IV VLSI IMPLEMENTATION OF NEURAL NETWORKS 9

Processing element model, PE row, PE array design, Processing element tile design, Direct, FFT-based, Winograd-based, Matrix multiplication based csonvolutional strategies, architectures for low-energy support vector machines.

UNIT V VLSI ARCHITECTURE FOR DEEP NEURAL NETWORKS 9

VLSI architecture for deep neutral networks, data and instruction flow in 2D systolic array architecture, Processing optimization in 2D systolic array, Pruning, compression , Hardware Accelerator.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

CO1: Ability to build hardware blocks for neurons model
CO2: Ability to implement machine learning techniques
CO3 : Ability to analyze digital implementations of Neural Network
CO4 : Ability to implement deep neural networks

Attested

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CO5: Ability to design energy-efficient machine learning hardware for deep neural network models

REFERENCES:

1. Bishop, C. (2006). Pattern Recognition and Machine Learning. Berlin: Springer-Verilog.
2. Ethem Alpaydin, Introduction to Machine Learning, PHI
3. Jose G. Delgado-Frias, William R. Moore, "VLSI For Artificial Intelligence And Neural Networks", Springer Science Business Media, LLC, 2001.
4. Mohamed I. Elmasry, "VLSI Artificial Neural Networks Engineering", Springer Science Business Media, LLC, 2000.
5. Sied Mehdi Fakhraie, Kenneth C. Smith, "VLSI - Compatible Implementations for Artificial Neural Networks", Springer Science Business Media, LLC, 1996
6. Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds. Machine Learning in VLSI Computer-Aided Design. Springer, 2019. VLS 5234: Physical D

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3	3	1	
CO2	2		3	3	1	
CO3	2		3	3	1	
CO4	2		3	3		
CO5	2		3	3		

VL3054 **MEMS AND NEMS** **L T P C**
3 0 0 3

UNIT I INTRODUCTION AND FABRICATION OF MEMS 9

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro-accelerometers and Micro fluidics, Materials for MEMS: Silicon, silicon compounds, polymers, metals. Photolithography, Ion Implantation, Diffusion, Oxidation, Dry and wet etching, Bulk Micromachining, Surface Micromachining, LIGA

UNIT II INTRODUCTION AND FABRICATION OF NEMS 9

Introduction to NEMS, Nano scaling, classification of nano structured materials, Applications of nanomaterials. Synthesis routes – Bottom up and Top down approaches.

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation

UNIT III DESIGN OF MEMS SENSORS AND ACTUATORS 9

Acoustic sensor – Quartz crystal microbalance, Surface acoustic wave, Flexural plate wave, shear horizontal; Vibratory gyroscope, Pressure sensors, Electrostatic actuators, piezoelectric actuators, Thermal actuators, Actuators using shape memory alloys, Microgrippers, Micromotors, Microvalves, Micropumps.

Attested

UNIT IV NEMS MATERIALS AND SENSORS 9

Quantum dots, Carbon nanotubes, Nanocrystalline ZnO, Nanocrystalline Titanium Oxide, Multilayered Films, Quantum well infrared photodetectors.

UNIT V INTRODUCTION TO OPTICAL AND RF MEMS 9

Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF MEMS – design basics, case study – Capacitive RF MEMS switch, performance issues.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course student will be able to:

CO1:Recognize the basics of materials and fabrication of micro electromechanical systems.
CO2:Devise the fabrication techniques of nano electromechanical systems
CO3:Analyze the key performance aspects of micro electromechanical sensors and transducers.
CO4:Analyze various aspects of nano materials and sensors.
CO5:Identify the potential applications of MEMS in the RF and optical domain

REFERENCES:

1. Ran Hsu, MEMS and Microsystems Design and Manufacture, Tata McGraw Hill, 2002.
2. Murty B.S, Shankar P, Raj B, Rath, B.B, Murday J, Textbook of Nanoscience and Nanotechnology, Springer publishing, 2013
3. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures”, CRC Press, 2002
4. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006.
5. Vinod Kumar Khanna Nanosensors: Physical, Chemical, and Biological, CRC press, 2012.
6. Mahalik N P, MEMS, Tata McGraw Hill, 2007.
7. Manouchehr E Motamedi, MOEMS: Micro-Opto-Electro-Mechanical Systems, SPIE press, First Edition, 2005.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	2		
CO2			3	2		
CO3	1		3	3		
CO4	1		3	2	1	1
CO5			3	3		

VL3011 MIXED SIGNAL IC DESIGN L T P C

3 0 0 3

UNIT I REFERENCE CIRCUITS 9

Performance Metrics, Current Mirrors, Self Biased Current Reference, startup circuits, VBE based Current Reference, VT Based Current Reference, Band Gap Reference , Supply Independent

Biasing, Temperature Independent Biasing, PTAT and CTAT Current Generation, Constant Gm Biasing.

UNIT II LOW DROP OUT REGULATORS 9

Performance Metrics, Shunt regulator, Error amplifier, AC Design, Stability, Internal and Externa Compensation, PSRR – Internal and External compensation circuits, NMOS vs. PMOS regulators.

UNIT III FREQUENCY SYNTHESIZERS 9

Integer-N Phase Lock Loop(PLL), Fractional-N Phase Lock Loop, Delay-Lock Loop (DLL), multiplying-DLL, Injection-locked PLLs, and Sub-sampled PLLs.

UNIT IV ACTIVE FILTER DESIGN 9

Butterworth Filter approximations, Chebyshev Filter approximations, Frequency Transformations, Continuous time filters- Biquad and Ladder based designs, Active RC and Gm-C Filters, Switch Capacitor Filters, Integrator realization and nonidealities.

UNIT V CLOCK AND DATA RECOVERY CIRCUITS 9

Channel characteristics-intersymbol interference, eye diagrams, Linear equalization at the transmitter and receiver; CDR Architectures, Trans Impedance Amplifiers, Linear Half Rate CDR Circuits, Wide capture Range CDR Circuits.

TOTAL : 45 PERIODS

COURSE OUTCOMES:

The student who undergoes this course will be able to

CO1: Design Band gap reference circuits.
CO2: Design Low Drop Out regulator for a given specification
CO3: Design Frequency synthesizers meeting a given specification.
CO4: Choose active filter topology and design for a given specification
CO5: Design clock generation circuits in the context of high speed I/Os, High speed Broad Band Communication circuits and Data Conversion Circuits.

REFERENCES:

1. Gabriel.A. Rincon-Mora, "Voltage references from diode to precision higher order bandgapcircuits", Johnwiley& Sons, Inc 2002.
2. Gabriel.A. Rincon-Mora, "Analog IC Design With Low-Dropout Regulators",McGraw-Hill Professional Pub, 2nd Edition, 2014
3. Floyd M. Gardner ,"Phase Lock Techniques" John wiley& Sons, Inc 2005.
4. R. Best, Phase-Locked Loops : "Design, Simulation, and Applications", McGraw Hill, 2003.
5. Williams and Taylor, "Electronic Filter Design Handbook", McGraw-Hill, 3rd Edition, 1995
6. Deliyannis, Sun, and Fidler, "Continuous-Time Active Filter Design", CRC Press 1998,
7. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001.

Articulation Matrix:

	PO1	PO2	PO3	PO4	PO5	PO6
CO1			2	2		
CO2			3	2		

CO3	1		3	3		
CO4	1		3	2	1	1
CO5			3	3		